



X-1069 US
10/086,129

PATENT
Conf. No.: 2232

IN THE UNITED STATES PATENT OFFICE

Applicant: David P. Schultz
Assignee: Xilinx, Inc.
Title: Method and System for Flexibly Nesting JTAG TAP
Controllers for FPGA-Based System-On-Chip (SoC)
Serial No.: 10/086,129 File Date: 2/28/2002
Examiner: James C. Kerveros Art Unit: 2133
Docket No.: X-1069 US Conf. No.: 2232

~~Do Not~~
~~ENTER~~
~~9/8/05~~

Mail Stop AF
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

AMENDMENT IN RESPONSE TO FINAL OFFICE ACTION

Dear Sir:

In response to the final rejection in the Office Action mailed from the Patent Office on June 14, 2005, please amend the claims as follows.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 8 of this paper.